HW

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,763	09/17/2003	Kent A. Dickey	10002827-2	1746

7590 03/16/2005

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MASKULINSKI, MICHAEL C	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,763	DICKEY ET AL.	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *1-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-37,39 and 40* is/are rejected.

7)☒ Claim(s) *38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/22/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Non-Final Office Action

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 21, 22, 23, 26, and 29-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-6 of U.S. Patent No. 6,651,193 B1.

Referring to claim 21, U.S. Patent 6,651,193 B1 discloses in claim 1 a distributed high performance coherent memory module with error containment, comprising:

a reading module for reading an error indication included in a packet reflective of a current state of a unit;

a determination module for determining if said state of a unit is in error mode;

a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode;

a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode;

a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode;

a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode;

a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit;

and means for moving said error indication coextensive only with errors in particular data.

However, U.S. Patent 6,651,193 B1 discloses additional limitations not in claim 21, and U.S. Patent 6,651,193 B1 does not disclose a method for providing a distributed high performance coherent memory with full error containment. It would have been obvious to one of ordinary skill at the time of the invention to omit the limitations in U.S. Patent 6,651,193 B1 and to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because the omission of these limitations in claim 21 of the instant application is an obvious expedient since the remaining limitations in claim 1 of the U.S. Patent 6,651,193 B1 perform the same function as the limitations in claim 21 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)). Further, to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 22, U.S. Patent 6,651,193 B1 discloses in claim 1 a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 23, U.S. Patent 6,651,193 B1 discloses in claim 2 a passing module for ensuring that each member of a group of connected units passes said error indication included in said packet, if said current state of a unit is in error mode, to a next unit member of group of connected units having at least one connected unit. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for ensuring that each member of said group of connected units having at least one connected unit passes said error indication included in said packet if said current state of a unit is in error mode to a next member of said group of connected units. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because

to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 26, U.S. Patent 6,651,193 B1 discloses in claim 4 a processor recovery module for implementing a recovery routine by said subject processor. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for implementing a recovery routine by said subject processor. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 28, U.S. Patent 6,651,193 B1 discloses in claim 5 a unit recovery module for implementing a software recovery routine to clear said error mode from said unit. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for implementing a software recovery routine to clear said error mode. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 29, U.S. Patent 6,651,193 B1 discloses in claim 6 a shared memory error module for setting a shared memory error bit to be included in said packet

for representing the presence of an error in a shared memory area. However, U.S. Patent 6,651,193 B1 doesn't disclose a method step for setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 31, U.S. Patent 6,651,193 B1 discloses in claim 6 a shared memory error module for setting a shared memory error bit to be included in said packet for representing the presence of an error in a shared memory area. However, U.S. Patent 6,651,193 B1 doesn't disclose a method wherein said error bit is provided as a shared memory bit, and wherein said unit comprises a shared memory area. It would have been obvious to one of ordinary skill at the time of the invention to have a method for performing the same function as the apparatus in U.S. Patent 6,651,193 B1. A person of ordinary skill in the art would have been motivated to make the modifications because to have a method for performing the same function as the apparatus would be obvious because an apparatus is nothing more than a method being implemented.

Referring to claim 32, U.S. Patent 6,651,193 B1 discloses in claim 1 a distributed high performance coherent memory module with error containment, comprising:

a reading module for reading an error indication included in a packet reflective of a current state of a unit;

a determination module for determining if said state of a unit is in error mode;

a permission module for permitting a set of network traffic to operate in a normal state if said state of said unit is not in error mode;

a driving module for driving an error indicator to a subject processor if said state of said unit is in error mode;

a blocking module for ensuring that a set of corrupt traffic does not reach I/O devices if said current state of unit is in error mode;

a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode;

a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit;

and means for moving said error indication coextensive only with errors in particular data.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent 6,651,193 B1 includes all of the limitations in claim 32 of the instant application. With regard to the additional limitations in claim 1 of U.S. Patent 6,651,193 B1, which are not included in claim 32 of the instant application, the omission of these limitations in claim 32 of the instant application is an obvious expedient since the remaining limitations in claim 1 of the U.S. Patent

6,651,193 B1 perform the same function as the limitations in claim 32 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claims 33-37, U.S. Patent 6,651,193 B1 discloses the limitations of claims 33-37 in claims 2-6 respectfully. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 2-6 of U.S. Patent 6,651,193 B1 includes all of the limitations in claims 33-37 of the instant application. With regard to the additional limitations in claims 2-6 of U.S. Patent 6,651,193 B1, which are not included in claims 33-37 of the instant application, the omission of these limitations in claims 33-37 of the instant application is an obvious expedient since the remaining limitations in claims 2-6, respectfully, of the U.S. Patent 6,651,193 B1 perform the same function as the limitations in claims 33-37, respectfully, of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claim 38, U.S. Patent 6,651,193 B1 in claim 1 discloses a shared memory bit module therein for providing a shared memory bit within said error indication and further comprising a shared memory area within said unit; and means for moving said error indication coextensive only with errors in particular data. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent 6,651,193 B1 includes all of the limitations in claim 38 of the instant application. With regard to the additional limitations in claim 1 of U.S. Patent 6,651,193 B1, which are not included in claim 38 of the instant application, the omission of these limitations in claim 38 of the instant application is an obvious expedient since the remaining limitations in claim 1 of U.S. Patent 6,651,193 B1 perform the same

function as the limitations in claim 38 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. Claim 23 recites the limitation "ensuring that each member of **said** group of connected units" in line 15. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 21, 24-31, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Gillett, Jr. et al., U.S. Patent 6,295,585 B1.

Referring to claim 21:

a. In the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the

nodes includes a local memory, which further comprises a shared memory (high performance coherent memory).

b. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (reading an error indication included in a packet, reflective of a current state of a unit; determining if said current state of said unit is in error mode). Further, in column 8, in Table 1, Gillett, Jr. et al. disclose that the STAE bit is part of a packet of bits.

c. In column 8, lines 31-55, Gillett, Jr. et al. disclose that the system operates normally unless the STAE bit is set (permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode).

d. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the

network, will stop transmission once it has detected the error (driving an error indicator to a subject processor if said current state of unit is in error mode).

e. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. Further, in column 14, lines 40-42, Gillett, Jr. et al. disclose that by halting data transmission from a faulty node, faulty data is not propagated to other nodes in the system (ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode).

Referring to claim 24, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said error indication in said packet is in the form of an error bit).

Referring to claim 25, in column 9, lines 24-28, Gillett, Jr. et al. disclose that the MC header includes various information received from the page control table entry (said error indication in said packet contained within a header of said packet).

Referring to claims 26 and 28, in column 10, lines 25-29, Gillett, Jr. et al. disclose that the hardware provides certain basic structural elements that ensure adequate software control of the structure, such as guaranteeing that order on the data link is preserved, providing loop-back capability, and terminating transmission to facilitate quick handling of errors (implementing a software recovery routine by said subject processor).

Referring to claim 27, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said reading step includes reading said error indication from an error bit).

Referring to claims 29 and 31, in the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared

memory. Further, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set. Thus the error bit that is set is in response to an error in shared memory (setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area).

Referring to claim 30, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (said error bit is provided as a fatal error bit).

Referring to claim 39, in column 9, lines 24-28, Gillett, Jr. et al. disclose that the MC header includes various information received from the page control table entry

(means for transporting error indications together with data which is in error). Further, in Figure 8, Gillett, Jr. et al. disclose that the header is sent with the data. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (means at each device to which such error data is directed and controlled in part by said error indicators for containing within said device said error data).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 22, 23, 32-37, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillett, Jr. et al., U.S. Patent 6,295,585 B1, and further in view of Hornung, U.S. Patent 6,175,931 B1.

Referring to claim 22, in column 9, lines 46-48, Gillett, Jr. et al. disclose that an arbitration protocol is implemented to ensure that each node in the network 'sees' the writes to the data link in the same order. However, Gillett, Jr. et al. don't explicitly disclose ensuring that each member of a group of connected units, reads said error indication included in said packet, if said current state of a unit is in error mode. In the Abstract, Hornung discloses an error propagation system and method uses a central control point at each node of a multinodal computer system to control error message distribution. It would have been obvious to one of ordinary skill at the time of the invention to include the error propagation system of Hornung into the system of Gillett, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because error notification and propagation provides the other nodes in the system important information. *An example of this situation is a simple timeout at a particular node. The local node detects the timeout error and logs it. In the meantime, a remote node could also be attempting to access that same memory location. The remote node then also will log a timeout error. From the perspective of the remote node, it is not easy to know if the memory at the target node is not working properly or if the linkage connecting the remote node to the target memory is not functioning properly* (see Hornung: column 1, lines 21-29).

Referring to claims 23 and 33, in column 9, lines 46-48, Gillett, Jr. et al. disclose that an arbitration protocol is implemented to ensure that each node in the network 'sees' the writes to the data link in the same order. However, Gillett, Jr. et al. don't explicitly disclose ensuring that each member of a group of connected units having at

least one connected unit passes said error indication included in said packet if said current state of a unit is in error mode to a next member of said group of connected units. In the Abstract, Hornung discloses an error propagation system and method uses a central control point at each node of a multinodal computer system to control error message distribution. Further, in column 2, lines 13-16, Hornung discloses that the error message can be passed between nodes with a single bit mapped into a high priority protocol on the SCI internodal link. It would have been obvious to one of ordinary skill at the time of the invention to include the error propagation system of Hornung into the system of Gillett, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because error notification and propagation provides the other nodes in the system important information. *An example of this situation is a simple timeout at a particular node. The local node detects the timeout error and logs it. In the meantime, a remote node could also be attempting to access that same memory location. The remote node then also will log a timeout error. From the perspective of the remote node, it is not easy to know if the memory at the target node is not working properly or if the linkage connecting the remote node to the target memory is not functioning properly* (see Hornung: column 1, lines 21-29).

Referring to claim 32:

a. In the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared memory (high performance coherent memory).

b. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (a reading module for reading an error indication included in a packet, reflective of a current state of a unit; determination module for determining if said current state of said unit is in error mode). Further, in column 8, in Table 1, Gillett, Jr. et al. disclose that the STAE bit is part of a packet of bits.

c. In column 8, lines 31-55, Gillett, Jr. et al. disclose that the system operates normally unless the STAE bit is set (permission module for permitting a network traffic set to operate in a normal state if said current state of a unit is not in error mode).

d. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will

stop transmission once it has detected the error (a driving module for driving an error indicator to a subject processor if said current state of unit is in error mode).

e. In column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. Further, in column 14, lines 40-42, Gillett, Jr. et al. disclose that by halting data transmission from a faulty node, faulty data is not propagated to other nodes in the system (a blocking module for ensuring that corrupt traffic set does not reach an I/O device if said state of said unit is in error mode).

f. In column 9, lines 46-48, Gillett, Jr. et al. disclose that an arbitration protocol is implemented to ensure that each node in the network 'sees' the writes to the data link in the same order. However, Gillett, Jr. et al. don't explicitly disclose a second reading module for ensuring that each member of a group of connected units reads said error indication included in said packet, if said state of said unit is in error mode. In the Abstract, Hornung discloses an error propagation system and method uses a central control point at each node of a multinodal computer system to control error message distribution. Further, in column 2, lines 13-16, Hornung discloses that the error message can be passed between nodes with a single bit mapped into a high priority protocol on the SCI internodal link. It would have been obvious to one of ordinary skill at the time of

the invention to include the error propagation system of Hornung into the system of Gillett, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because error notification and propagation provides the other nodes in the system important information. *An example of this situation is a simple timeout at a particular node. The local node detects the timeout error and logs it. In the meantime, a remote node could also be attempting to access that same memory location. The remote node then also will log a timeout error. From the perspective of the remote node, it is not easy to know if the memory at the target node is not working properly or if the linkage connecting the remote node to the target memory is not functioning properly* (see Hornung: column 1, lines 21-29).

Referring to claim 34, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set (an error indication module for providing an error indication to be included in said packet reflective of the current state of a unit).

Referring to claims 35 and 36, in column 10, lines 25-29, Gillett, Jr. et al. disclose that the hardware provides certain basic structural elements that ensure adequate software control of the structure, such as guaranteeing that order on the data link is preserved, providing loop-back capability, and terminating transmission to facilitate quick handling of errors (implementing a software recovery routine by said subject processor).

Referring to claim 37, in the Abstract, Gillett, Jr. et al. disclose a multi-node computer network that includes a plurality of nodes coupled together via a data link. Each of the nodes includes a local memory, which further comprises a shared memory. Further, in column 8, lines 50-55, Gillett, Jr. et al. disclose that when the Suppress Transmit After Error (STAE) bit is set, any write to the corresponding page of Memory Channel (MC) address space from a node that has detected an error at some point during the transaction of the data to another node in the network, will stop transmission once it has detected the error. And in column 8, lines 65-67 continued in column 9, lines 1-2, Gillett, Jr. et al. disclose that when the Suppress Receive After Error (SRAE) bit is set, if an error occurs during the receipt of a write to the page from the cluster, the MC adaptor at the receiving node will stop accepting data to the page for which this bit is set. Thus the error bit that is set is in response to an error in shared memory (setting a shared memory error bit to be included in said packet as representative of a presence of an error in a shared memory area).

Referring to claim 40, in column 9, lines 46-48, Gillett, Jr. et al. disclose that an arbitration protocol is implemented to ensure that each node in the network 'sees' the

writes to the data link in the same order. However, Gillett, Jr. et al. don't explicitly disclose means fro propagating said error indications to next ones of said devices to which said error data must be delivered, said propagating occurring concurrently with error data delivery. In the Abstract, Hornung discloses an error propagation system and method uses a central control point at each node of a multinodal computer system to control error message distribution. Further, in column 2, lines 13-16, Hornung discloses that the error message can be passed between nodes with a single bit mapped into a high priority protocol on the SCI internodal link. It would have been obvious to one of ordinary skill at the time of the invention to include the error propagation system of Hornung into the system of Gillett, Jr. et al. A person of ordinary skill in the art would have been motivated to make the modification because error notification and propagation provides the other nodes in the system important information. *An example of this situation is a simple timeout at a particular node. The local node detects the timeout error and logs it. In the meantime, a remote node could also be attempting to access that same memory location. The remote node then also will log a timeout error. From the perspective of the remote node, it is not easy to know if the memory at the target node is not working properly or if the linkage connecting the remote node to the target memory is not functioning properly* (see Hornung: column 1, lines 21-29).

Allowable Subject Matter

9. Claim 38 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100